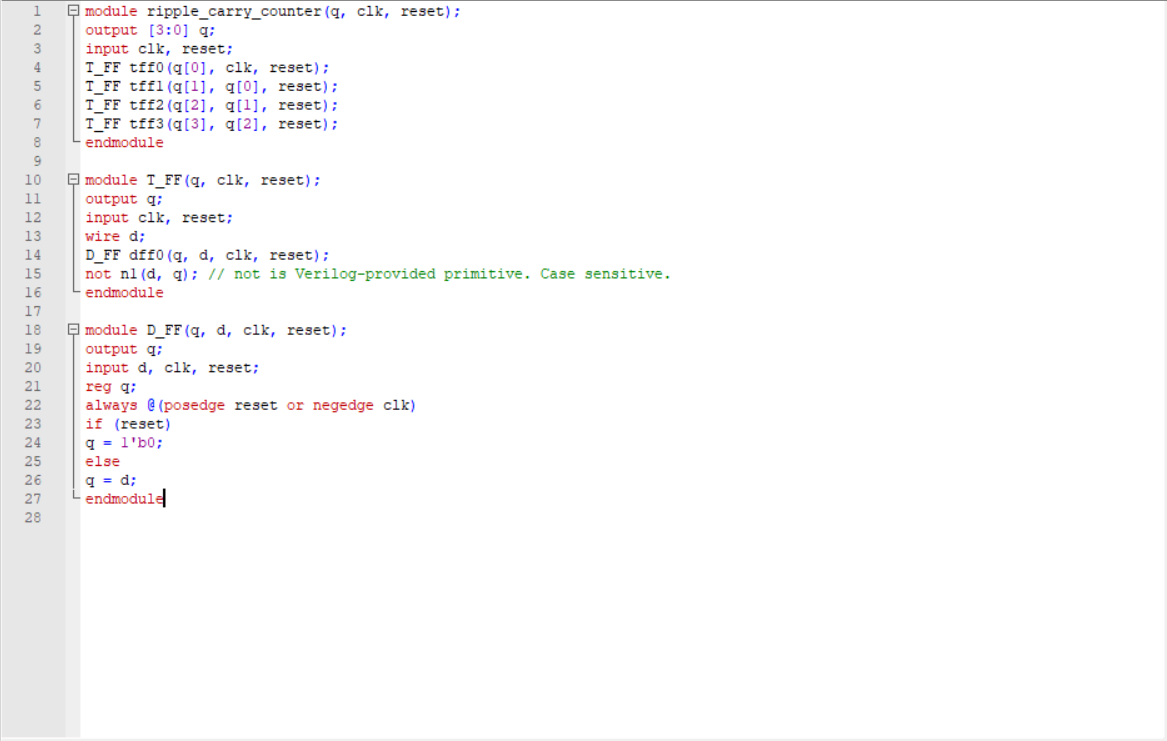
**Ripple carry counter**

Counter is basically used to count the number of clock pulses applied to a flip flop.

Ripple counter is a cascaded arrangement of flip-flops drives the clock input of the following flip-flop. The number of flip flops in the cascaded arrangement depend on the num off different logic states it goes through before repeating the sequence a parameter known as the modulus of the counter.

**Verilog code**:

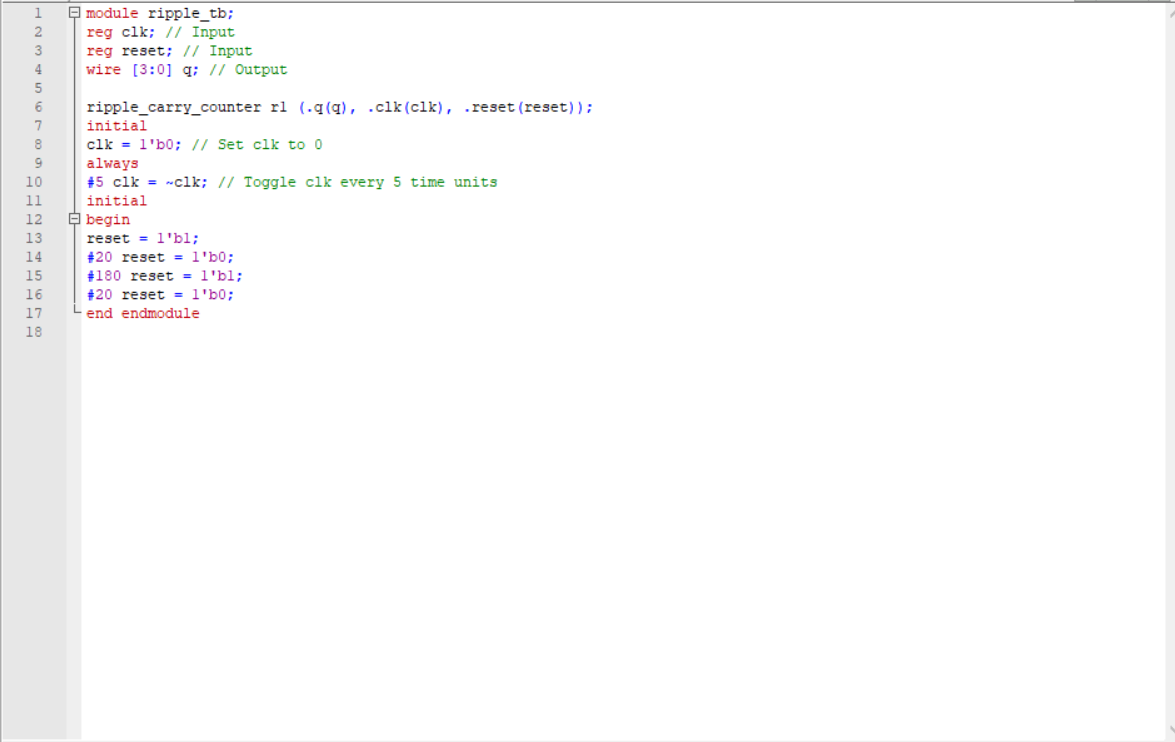


Comments:

//Line 4 to 7: Initiate 4 TFF to update the count of the counter system

// Line 10 to 15: Declare Tff module where tff takes clk and rest as input and q is the output. In here wwe instantiate d flip flop and not gate as t flip flop part

**Testbench**:



Comment:

// We set the initial clk to be 0 and the step for clock toggle is 5ns

// This we provide reset values as the input where reset =1’b1, continue with re = 0,1,0,…

**Wave form**: 